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An optimized phase-shifted full-bridge converter for wide input voltage range

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ABSTRACT

Zero-voltage phase-shifted full-bridge converters (PSFB ZVS) have been widely used in the high frequency, high power applications with these characteristics of zero-voltage switching (ZVS) by Phase shifting based on the fixed frequency. However，the load and input voltage range for full power transistors realizing ZVS are limited. So this paper proposes a solution with adding a coupled inductor on the primary side of transformer，as well as adopting active clamping topology on the secondary side. The auxiliary circuit can achieve adaptive energy storage by the processor，make the input voltage range and load range of ZVS of all switching tubes greater, reduce the circulation and conduction losses, minimize the duty cycle of secondary loss problems.

KEYWORDS

PSFB; ZVS; Active clamping.

INTRODUCTION

Phase-Shift Full-Bridge Zero-Voltage Switched (PSFB ZVS) has been widely used in high frequency, high power applications because of its such as without external components and achieve zero voltage switching (ZVS), the frequency characteristics of fixed and simple control etc.[1] But ifthe inductor or leakage in the high frequency transformer primary side connected in series is not large enough, or no additional external auxiliary inductance, ZVS realized the full power tube limited by the voltage range of load and input. When to achieve ZVS under light load by increasing the inductance to store energy also have adverse effects. Including the missing duty cycle of secondary side increases, it caused more serious parasitic oscillation by the parasitic junction capacitance and leakage inductance of the transformer rectifier diode resonant[2].

In order to ensure that the duty cycle of the secondary side as small loss and parasitic oscillations, thus optimizing the performance of the phase-shift full-bridge zero-voltage switched, Presented by literature[3-6] schemes are generally use stored in the auxiliaryinductor in power for all of the primary side switch tube in the larger load and inputvoltage range to provide the ZVS environment, The ideal state is when fully loaded conditions, the load current is large can store enough energy in converter inductance element to ensure that all of the power to beZVS, The load current is reduced, the auxiliary circuit should be added to the maintain inductance energy of ZVS until the no-load can achieve maximum inductance energy required for ZVS. The literature[3] and[4] using stored the energy in the magnetizing inductance of the auxiliary transformer to extend the range of ZVS, the energy to achieve ZVS in the proposed scheme is increased with thegrowth of the input voltage, So, the energy in order to realize the ZVS and stored is independent of load, it can not be caused by the optimal balance between the loss of ZVS achieved within the confines of the full load and loss of auxiliary circuit. In the literature[5,6] is introduced using the auxiliary circuit stored energy at full range of the load. the maindisadvantage that produce larger circulation when no load is to achieve ZVS to affect the efficiency of the converter.

This paper combines a variety of improved phase shifted full bridge topology[7,8], Proposed add a coupled inductor at the primary side, the improved structure of the active clamp at the secondary side, Additional auxiliary circuit on the primary side can realize the adaptive energy storage, it can achieve all switches of ZVS in a widely range of input voltage and larger load range and reduce the circulation and conduction losses, In addition, because the presence of coupling inductance does not need too many of the leakage inductance of the transformer, this can make the high frequency transformer leakage inductance is minimized which greatly reduce the loss of duty cycle at the secondary side. This article has carried on the analysis about the active clamp at the secondary side to significantly suppress the surge voltage on the rectifier diodes. Finally, the correctness and practicability of the new topology is analyzed through experiments, and gives the corresponding conclusions.

PRINCIPLE ANALYSIS AND PARAMETER DESIGN OF FULL BRIDGE PHASE SHIFT WITH COUPLED INDUCTORS

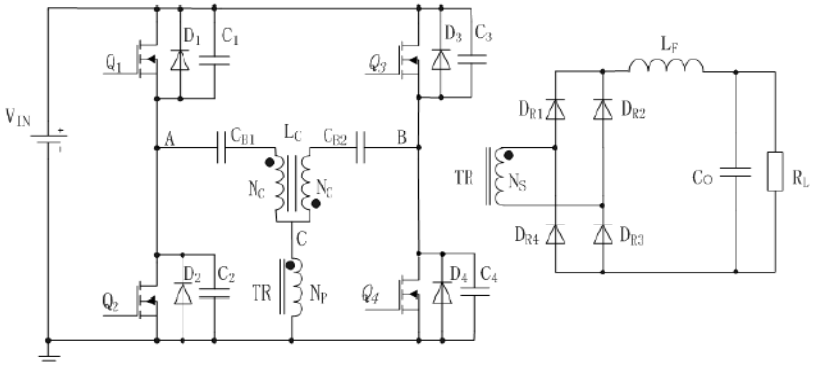


Figure 1: Phase-shift full-bridge zero-voltage switched with coupled inductors

As shown in Figure 1, the range of ZVS at the power tube on the primary side extended by the phase shifted full bridge zero voltage switched with an additional coupling inductance on the primary side. In order to avoid saturation about high-frequency transformer and coupled inductor core, it connect two isolation capacitors to block DC component in the both of primary side.

A simplified circuit diagram shown in Figure 2, to facilitate the analysis of the modal of the circuit diagram, make the following assumptions:

All switches, diodes, inductors and capacitors are ideal device;

Secondary side output filter inductors are large enough, which are equivalent to a constant current source with amplitude of I_0 in a switching period;

Isolating capacitor C_{B1} and C_{B2} are large enough, which are equivalent to a constant current source in a switching period. Furthermore, since the average voltage of the windings of the coupled inductor and transformer windings is zero in a

switching period; Each of the pair of power transistor in each arm of the bridge is turned on 50% of the switching period, the amplitude of voltage source V_{CB1} and V_{CB2} is $V_{IN}/2$;

Ignore the leakage inductance of coupled inductors and high-frequency transformer and the transformer magnetizing inductance.

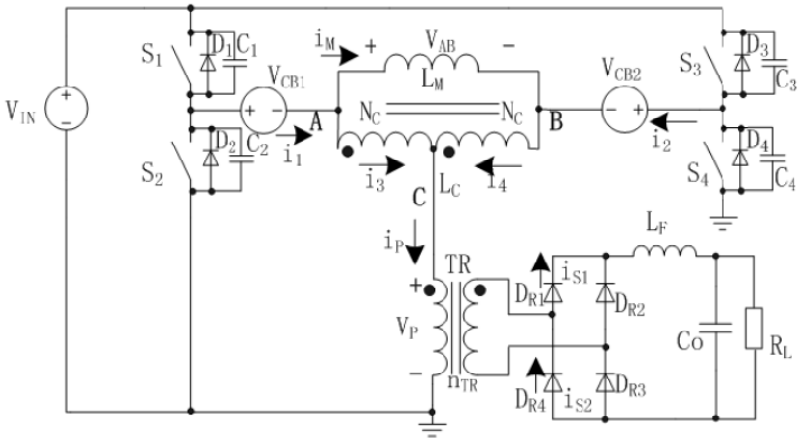


Figure 2: Simplified equivalent circuit of full bridge phase shift with coupled inductors

Magnetizing inductance of coupled inductors L_C and parallel capacitor in primary side $C_1 - C_4$ play a important role in circuit. In Figure 2 coupled inductor L_C is equivalent to an ideal transformer whose turns ratio is 1, and the magnetizing inductance crossing in the windings. Each turns ratio is N_C. Equivalent circuit of each switching period is shown in Figure 3. Next, the analysis of each of switching modleis given.

State 0 [[t_0～t_1]]

At the t_1 moment, S_1 and S_2 switch on, i_1 and i_2 flow through the corresponding transistor、isolation capacitance、inductor winding and the primary side of high frequent transformer, the equivalent circuit is shown in Figure 3(a). In the same time, the secondary side load circuit I_0 flows through D_{R1} and D_{R3}, it is easy to know that $i_p = i_1 + i_2 = I_0 / n_{TR}$, where $n_{TR} = N_p / N_s$ is ratio of transformer, N_p and N_s is the turn number of primary and secondary side. Easy to know from Figure 3(a), the voltage of A、B point $V_{AB} = 0$, because voltage source V_{CB1} and V_{CB2} flow through S_1 and S_2 connecting in reverse. According to the enwsinding way of coupled inductor, $V_{AB} = V_{AC} + V_{CB} = 0$. Only in the moment of $V_{AC} = V_{CB} = 0$ that V_{AB} will remain in 0. Obviously the voltage of A、B、C point is same in that moment, so the primary side voltage $V_p = V_{IN} - V_{IN}/2 = V_{IN}/2$. Furthermore, the excitation current i_{CM} remains constant. Since the turn number ratio is 1, so the current of AC brunch i_3 is equal to the current of BC brunch i_4, can conclude that $i_1 = i_p/2 + i_M$ and $i_2 = i_p/2 - i_M$.

State 1[t_1～t_2]

In the t_1 moment, S_1 switch off, current i_1 trance from S_1 to its parallel capacitor C_1, as shown in Figure 3(b). In this moment, i_1 charge C_1 and discharge C_2, furthermore, their voltage sum is a constant input voltage V_{IN}. So with point A ‘s voltage rise., the voltage V_{AB} and V_p decline. Specifically speaking, the value of V_{AB} change from 0 to $-V_{IN}$, the value of V_p change from $V_{IN}/2$ to 0.

State 2[t_2～t_3]

When parallel capacitor C_2 discharge, it is to say the value of V_{S2} is 0. i_1 begin to flow through S_2‘ inverse parallel diodes D_2, as shown in Figure 3(c). Since the negative V_{IN} is applied between point A and B of coupled wingding,

which will cause excitation current i_M decline with a rate of $-V_{IN}/L_M$, however, in this state, primary side current i_p remains I_0/n_{TR}. Current $i_1 = i_p/2 + i_M$ decline and current $i_2 = i_p/2 - i_M$ rise simultaneously. To realize the ZVS opening of S_2, S_2 should be triggered immediately at the moment of V_{S2} decline to zero and before its inverse diodes switch off.

State 3[t_3～t_4]

In the t_3 moment, excitation current i_M decline to zero, then increase inverse, as shown in Figure 3(d). So i_1 decline and i_2 rise.

State 4[t_4～t_5]

In the t_4 moment, S_2 switch off cause that i_2 converter through C_3 instead S_3, as shown in Figure 3(e). While $_{C_3}$ charging, $_{C_4}$ are discharged at the same rate, the $_{S_3}$ voltage across the $_{V_{S3}}$ increased from 0 to $_{V_{IN}}$ while $_{V_{S4}}$ from the $_{V_{IN}}$ fell to zero. At this stage, the voltage at point B drop from $_{V_{IN}/2}$ to $_{-V_{IN}/2}$, the voltage at point A in the phase constant for $_{-V_{IN}/2}$, while voltage $_{V_{AB}}$ becomes 0 from $_{-V_{IN}}$. Primary side voltage from 0V reverse to $_{-V_{IN}/2}$ will force the secondary side rectification from $_{D_{R1}}$, $_{D_{R3}}$ commutation to $_{D_{R2}}$, $_{D_{R4}}$ path, If the coupled inductors $_{L_C}$、the leakage inductance of the transformer and other stray inductance is 0, Then the commutation process will be completed instantaneously, However, the actual amount of said inductor are present, the load current commutation process will take some time, and, from the beginning to the negative, secondary side rectification in order to ensure the load current, rectifier tube $_{D_{R1}-D_{R4}}$ will all be turned on, that at this time the transformer secondary winding in the short circuit state, that caused the loss of the duty cycle of the secondary issues.

Switch mode 5[t_5～t_6]

At time $_{t_5}$, and the switch $_{S_3}$ shunt capacitor $_{C_3}$ is fully charged, $_{S_3}$ voltage across $_{V_{S3}}$ reach $_{V_{IN}}$, while the tube voltage across $_{V_4}$ drop to 0, the current $_{i_2}$ will through $_{S_4}$ switch at both ends anti-parallel freewheeling diode, as shown in Figure 3(f). Because the secondary side is still in commutation process. Current $_{i_{S1}}$ flows $_{D_{R1}}$、$_{D_{R3}}$、rectifier is reduced, current $_{i_{S2}}$ flow through $_{D_{R2}}$、$_{D_{R4}}$ rectifier is rise, corresponds to the primary side current $i_P = (i_{S1} - i_{S2})/n_{TR}$, in the reverse direction when $_{i_{S2}}$ becomes greater than $_{i_{S1}}$. Moreover, to achieve the switch $_{S_4}$ is ZVS, to $_{S_4}$ on signal, after the required voltage value $_{V_{S4}}$ reduced to 0 and current $_{i_2}$ flows through the switch $_{S_4}$ anti-parallel diode phase.

Switch mode 6[t_6～t_7]

At time $_{t_6}$, load current commutation process has been completed, as shown in Figure 3(g), at this stage, the amount of current $_{i_P}$、$_{i_M}$、$_{i_1}$、$_{i_2}$ is constant and is reversed.

Switch mode 7[t_7～t_8]

At time $_{t_7}$, switch $_{S_2}$ is turned off, into the half- cycle of next stage of the switching, at the moment the switch $_{S_1}$ in parallel with the capacitor $_{C_1}$ begins to discharge at the same time in parallel with $_{S_2}$ the capacitor $_{C_2}$ charging, as shown in Figure 3(h). And the voltage $_{V_{AB}}$ between A and B in this period rose from 0 to $_{V_{IN}}$, primary side voltage $_{V_P}$ from $_{-V_{IN}/2}$ to 0.

Switch mode 8[t_8～t_9]

At time $_{t_8}$, the $_{V_{S2}}$ voltage across the switch $_{S_2}$ rises to, meanwhile $_{V_{S1}}$ voltage drops to 0 and anti-parallel diode $_{D_1}$ and $_{S_1}$ is turned on, as shown in Figure 3(i).

In order to realize the ZVS of the switch tube S_1, we should guarantee in V_{S1} drop to 0 and D_1 conduction phase to S_1 guide the number of communication. Because of the S_2 shutting off, the V_{AB} voltage value already starting from the moment on the stage of t_7 has gradually increased, resulting in A and B between excitation current i_M from A maximum negative polarity - i_M reduced to zero. At the t8 moment, the value of the V_{AB} reaches constantly on excitation inductance L_M, so i_M starts to VIN/LM change at a fixed rate.

Switch mode 9[t_9～t_{10}]

At the t_9 moment, the current i_M is from negative to zero, and Reverse to continue normal polarity increased, as shown in Figure 3(j). Because of $i_1=i_P/2+i_M$ and $i_2=i_P/2-i_M$, and the i_P remains constantly, the value of the i_1 current at the t_7

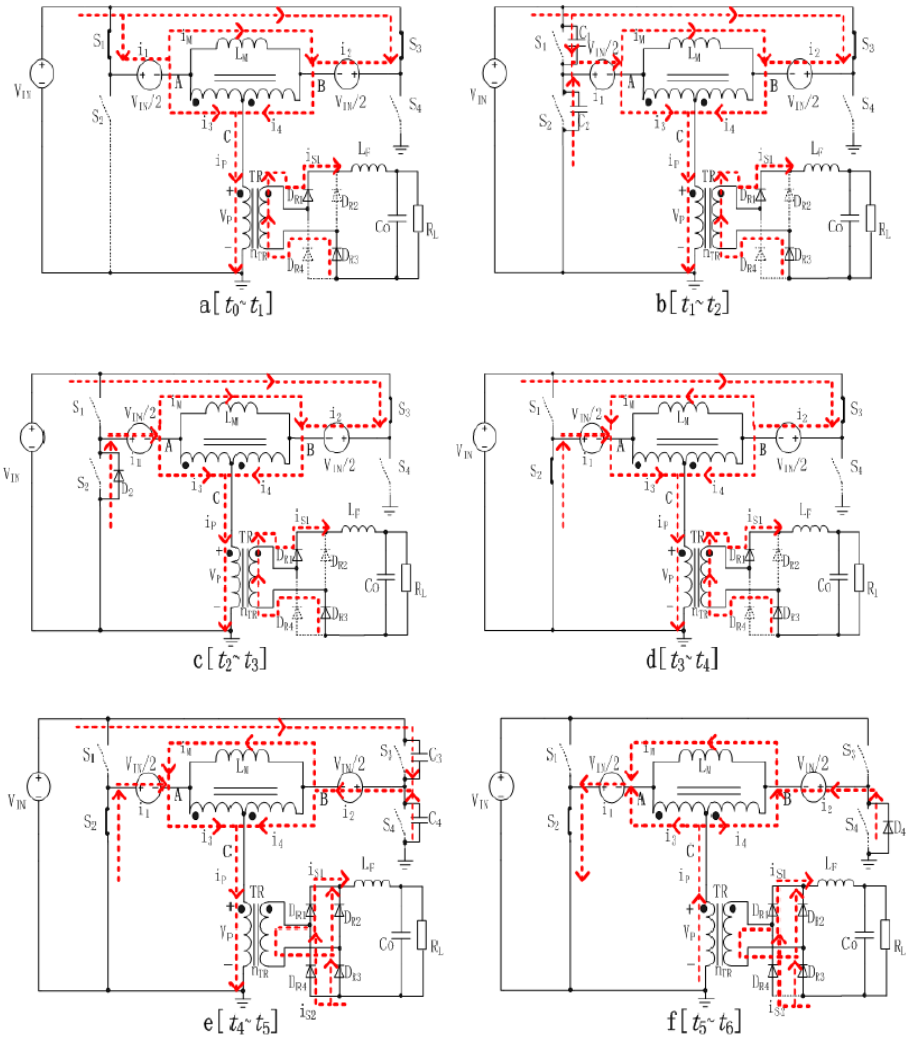
moment has already decreased from the negative moment and the i_2 current value at the t_7 moment has negatively increased, and in this time period is still change according to the original direction.

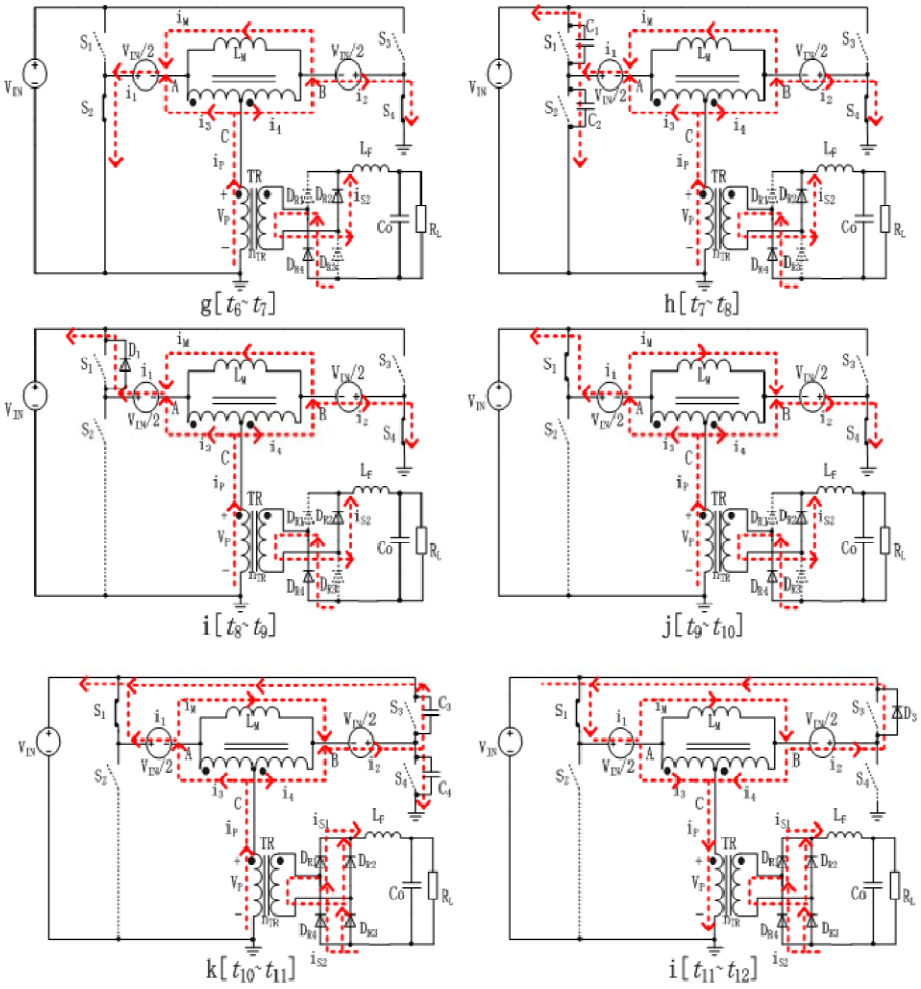
Switch mode 10[t_{10}～t_{11}]

The switch tube S_4 of shutting off in times of t_{10} cause before the current i_2 through the S_4 to shunt the capacitance C_4 converter, as shown in Figure 3(k). On parallel capacitance C_4 charging at the same time, the bridge arm of the parallel capacitance C_3 discharges at the same rate, so the potential of the point B is from VIN / 2 up for VIN / 2, the potential of the point A in this phase constants for VIN / 2, while the V_{AB} voltage value decreased from VIN to 0, then the original side voltage V_P rise from 0 for VIN /2. In this way, at the edge of the deputy rectifier side converter process will appear, as mentioned above, the difference is only when the VP into normal polarity from the beginning, vice side rectifier in order to ensure the load current, rectifier D_{R1} - D_{R4} will be all conducted, namely the deputy winding transformer is under short circuit.

Switch mode 11[t_{11}～t_{12}]

At the t_{11}moment, the shunt capacitance C_3 of the switch tube S_3 discharges completely, the S_3 both ends of the voltage V_{S3} reaches 0, at the same time, the voltage at the ends of the tube V_{S4} rises to VIN, then the current i_2 will stream by the S_3 switch tube on both ends of the parallel diode, as shown in Figure 3(l). Due to the deputy while still be in the process of converter, through the D_{R2}, D_{R4} rectifier current i_{S2} in reducing, and through the D_{R1}, D_{R3} rectifier current i_{S1} is on the rise, Corresponding to the original side current $i_P=(i_{S1}-i_{S2})/n_{TR}$, its direction in t_{11} moment when the $i_{S1} > i_{S2}$ becomes a positive. In order to realize ZVS switching tube S_3, we need after the V_{S3} voltage dropping to zero and the S_3 parallel diode D_3 conduction phase to S_1 guiding the number of communication. At the t_{12} moment, the vice edge process completed, the switch tube S_3 conducted, the equivalent circuit state was backed to the circuit shown in Figure 3(a), and a switch ended the working process of the cycle.





According to the modal analysis in the above, when the current i1=iP/2+iM maximum, the bridge arm switch tube S1-S2 begin to commutate; similarly, when the current i2=iP/2-iM maximum, the bridge arm switch tube S3-S4 begin to commutate. The advanced arm S1- S2 switch tube parallel capacitor charging and discharging of the energy needed by output filter inductance LF and former deputy side excitation inductance coupling inductance LC provide both; the lagging arm S3 - S4 switch tube parallel capacitor charging and discharging of the energy needed by the high frequency transformer leakage inductance of the LF excitation inductance coupling inductance and LC provide both. To be sure, the advanced arm S1-S2 can acquire energy that realize ZVS, the energy only can be needed from the output filter inductor LF and does not require too much energy deposited in the primary side coupling inductance; but lagging arm switch tube S3 - S4 to realize ZVS can only rely on the energy deposited in the coupled inductor in excitation inductance, high-frequency transformer leakage inductance in this paper the design is very small, it is mainly consider reduce pair of side duty cycle loss and parasitic oscillation.

In order to achieve the wide input voltage range and large power load range of ZVS, excitation inductance of coupling inductance is needed to meet the following formula:

$$\frac{1}{2}\cdot L_{M}\cdot I_{M}^{2}\geq C\cdot V_{IN}^{2}+\frac{1}{2}\cdot C_{LC}\cdot V_{IN}^{2}+\frac{1}{2}\cdot C_{TR}\cdot\left(\frac{V_{IN}}{2}\right)^{2} \quad (1)$$

Among them, C = C3 = C4 is the shunt capacitance values of switch tube, CLC is the winding capacitance of coupling inductance LC, CTR is winding capacitance of high-frequency transformer TR. When the CLC and CTR are ignored, it is simplified formula (2), we can known the inductance LM when no-load and the maximum input voltage, we can realize ZVS of the switch tube when full load and input voltage range in theory.

$$\mathrm{L}_{M}\cdot I_{M}^{2}\geq 2\cdot \mathrm{C}\cdot V_{IN}^{2} \quad (2)$$

I_M here can use formula (3) to determine, Including Deff is Vice edge of duty ratio. Ts is consider to be a of switching cycle, and f_S is for the switching frequency.

$$V_{IN} = L_M \cdot \frac{2 \cdot I_M}{(1 - D_{eff}) \frac{T_S}{2}} \quad \textbf{(3)}$$

Be near $$I_M = \frac{(1 - D_{eff}) \cdot V_{IN}}{4 \cdot L_M \cdot f_S} \quad \textbf{(4)}$$

Due to the no-load condition, lead and lag of Full-Bridge Converter's arm phase-out to vice edge that is duty ratio D=0, and Combined with the formula (2), (4) can get the determined the value of the LM under the no-load and maximum voltage input as shown in formula (5). in addition, For S1 and S2 bridge arm bearing current will be bigger than S3 - S4 bridge arm current. When the conduction phase coupling inductance current excitation inductance L_M and $i_M$there are differences. Therefore, should choose a maximum of L_M.

$$L_M \leq \frac{1}{32 \cdot C \cdot f_S^2} \quad \textbf{(5)}$$

This article uses the phase shifting full bridge topology structure, Excitation inductance coupling inductance value will have little impact on the primary side current commutation time. Reversing time is connected with the size of the leakage inductance of the transformer and the transformer. Due to the concatenated in main power circuit, Its value, the greater the turnaround time will be longer. And in order to reduce the vice and duty ratio and optimizing the circuit performance, It is necessary to reduce the leakage inductance of the transformer and the coupling inductance. It is the same to be weaken on the rectifier diode voltage oscillation problem.

VICE EDGE ACTIVE CLAMP MODE ANALYSIS AND PARAMETER DESIGN

There is a real diode stray capacitance of PF, The parasitic capacitance and leakage inductance of the transformer. Under the action of step signal is easy to generate oscillation[9]. In order to completely inhibit the rectifier diode voltage oscillation, In order to improve the phase shifting full bridge ZVS DC/DC. Switching frequency and power rating of the converter, This article adopts the way of active clamp. This method can completely inhibit on the rectifier diode voltage oscillation, The so-called active clamp that is between the diode rectifier side and to add a power switch tube and capacitance, Using capacitanceV_{rec} Voltage clamping. The capacitor should be greater than the size of the parasitic capacitance. The leakage inductance of the transformer and the clamping capacitance in resonance, With the source of the clamping topology structure of the whole bridge as shown in Figure 4, The leakage inductance and clamping capacitance resonance, filter inductance LF can be as a constant current source, Do not participate in the resonant., At this point in the leakage inductance of the current can be divided into the sum of harmonic current and load current, Due to the clamping capacitance is large enough, So the leakage inductance and clamping capacitance resonance cycle a lot., Set period of time in the Vrec., capacitance C_S of the of harmonic current can be seen as linear change., The switch of the sequential on clampingMOSFET. As shown in Figure 5.

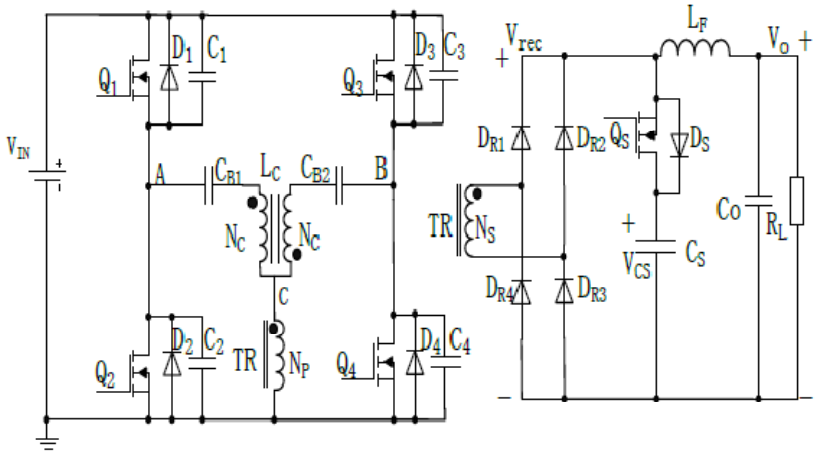


Figure 4: Vice edge active clamp with a new type of phase-shift full bridge ZVS of convertor

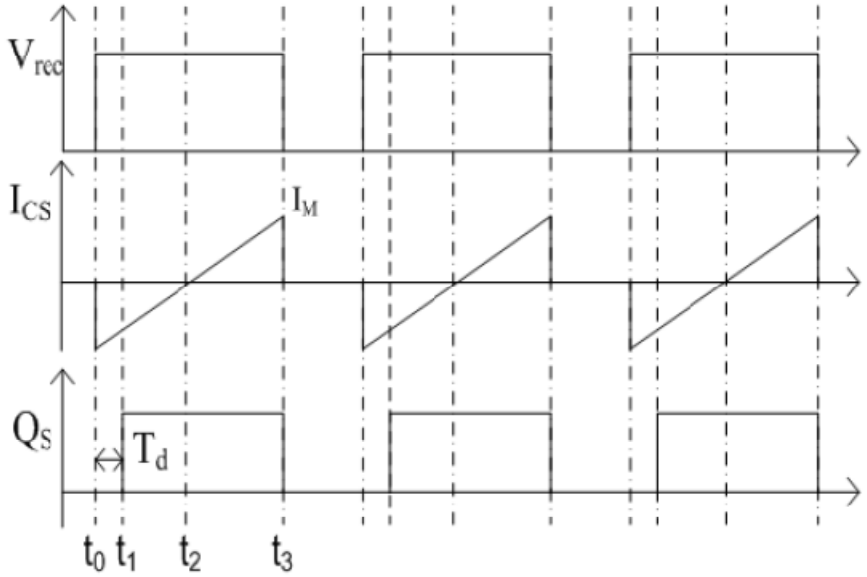


Figure 5: Secondary side of the transformer rectifier side clamping circuit of electric wave

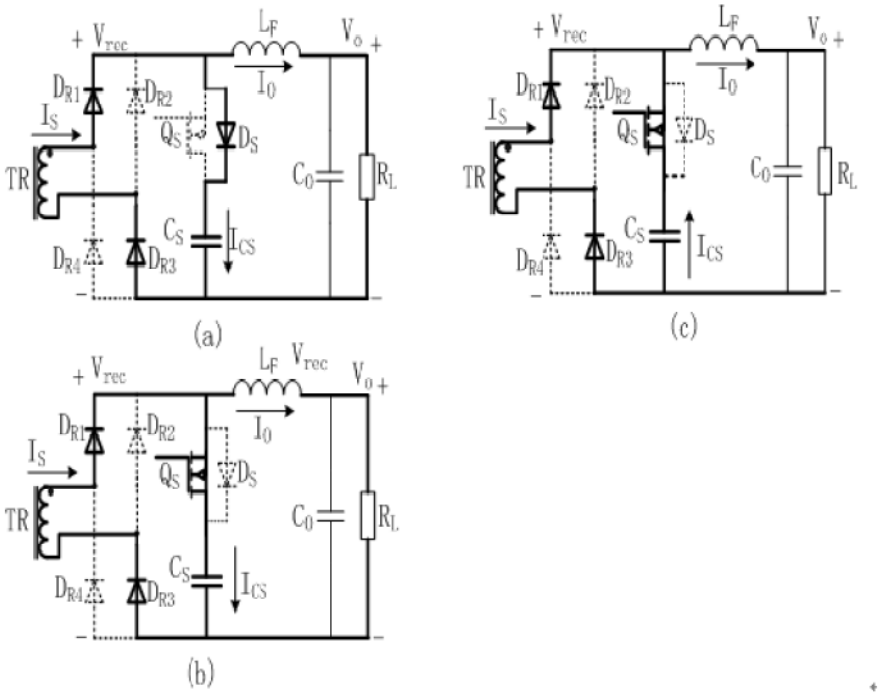


Figure 6: Some modal map secondary side of the transformer rectifier side clamp circuit

When it's steady state, clamp capacitor CS charge and discharge current average bound to zero in order to maintain steady-state voltage in one cycle. Figure 6, it shows the half of the duty cycle of a schematic view of the operating mode. Specific analysis is as follows:

Operational modal 1 (t_0~t_1)

Secondary voltage of the transformer has been established in this case. Figure 6(a) shows, But the switch of MOSFET has not yet opened. At this point the body diode through the MOSFET, the leakage inductance of the transformer, the parasitic capacitance of a diode and the clamp capacitor CS forms a resonant circuit. Or is CS absorbed the oscillation energy form transformer leakage inductance and parasitic capacitance.

Operational modal 2 (t_1~t_2)

MOSFET opening at time t1, Figure 6(b) shown, it shows direction of resonance current ICS constantsuntil to zero. This phase capacitor CS has been charged.

Operational modal 3 (t_2~t_3)

At time t2, ICS had zero, Current commutation, Clamp capacitor CS discharged. Figure 6(c) shown.

When the clamp capacitor CS chosen large enough, Steady-state voltage of capacitor VCS equal voltage of rectifier Vref, And for flat square wave. Vrec sizerelated output voltage duty cycle Deff, Leakage inductance Llk and the output voltage Vo. Reasonably determine the relevant parameter values, In order to reduce the rectifier voltage stress, Ensure VCS within the allowable voltage range. When the converter steady work, The average current flowing through the clamp capacitance CS is equal to zero, Therefore, ICS clamp current peak is determined according to the formula (6) - (8).

$$I_{CS} = \frac{1}{2} \cdot K \cdot D_{eff} \cdot \frac{T_S}{2} \tag{6}$$

$$k = \frac{K \cdot V_{IN} - V_{CS}}{K^2 \cdot L_{lk}} - \frac{V_{CS} - V_O}{L_F} \tag{7}$$

$$D_{eff} = \frac{V_O}{V_{CS}} \tag{8}$$

Here, The clamp capacitor current k is the slope, K is a constant.

By analyzing known clamp capacitor current reaches a peak moment, Corresponds to the leakage inductance Ilk and resonant voltage of the parasitic capacitance rectifier reaches steady-state voltage of the capacitor VCS moment

When the voltage gets VCS, according to the series resonance theory, I_{CS} is :

$$I_{CS} = \frac{K \cdot V_{IN}}{\sqrt{\frac{L_{lk}}{C_{sec}}}} \cdot \cos\left[\sin^{-1}\left(\frac{V_{CS} - K \cdot V_{IN}}{K \cdot V_{IN}}\right)\right] + 2 \cdot I_{rr} \tag{9}$$

In this formula, C_{sec} is the sum of rectifiertubestraycapacitance and distributedcapacitance of transformerwinding. I_{rr} is rectifiertube reverse recovery current. The steady state voltage V_{CS} of Clamping capacitance can be got from simultaneous above formulas. And the Simplified expression can be got inidealconditions of ignoring C_{sec} and I_{rr},

$$V_{CS} = \frac{K \cdot V_{IN} \cdot L_F}{L_F + K^2 \cdot L_{lk} \cdot (1 - D_{eff})} \tag{10}$$

Clamping capacitance $C_{S\,can}$ be got according to formula (11). The value of it is also based on the actual debugging situation and simulationresult.

$$\frac{\Delta V_{CS} \cdot L_F}{V_{CS} - V_O} = \frac{(D_{eff} \cdot T_S)^2}{8 \cdot C_S} \tag{11}$$

In this formula, ΔV_{CS} is magnitude of a voltage fluctuation on the capacitance, which is demanded to be $\frac{\Delta V_{cs}}{V_{cs}} \le 10\%$.

Circuittopology is proved by using experiments which is based on theoretical analysis. The experimental prototype parameter is: input voltage V_{IN}=125~195V, output voltage V_O=160±10V, load power P_L=5Kw.

As shown in Figure 7, when its input voltage is 160V, output voltage is 170V, and the load is 2Kw, it is midpoint voltage waveform of the bridge and primary-side voltage waveform. The slope of primary-side voltage waveform is the sum of the slope of the clamping capacitance current and the slope of the output filter inductor current. When its midpoint voltage waveform of the bridge V_{AB}=0, clamping MOSFET is closed, leading to the clamping capacitance current to be zero, which supplies power to the load. Because the value of output filter inductance is large, the current cannot change suddenly, primary-side current must supply a current to substitute camping capacitance current. Then the current i_P appears to be the phenomenon like steps in the figure.

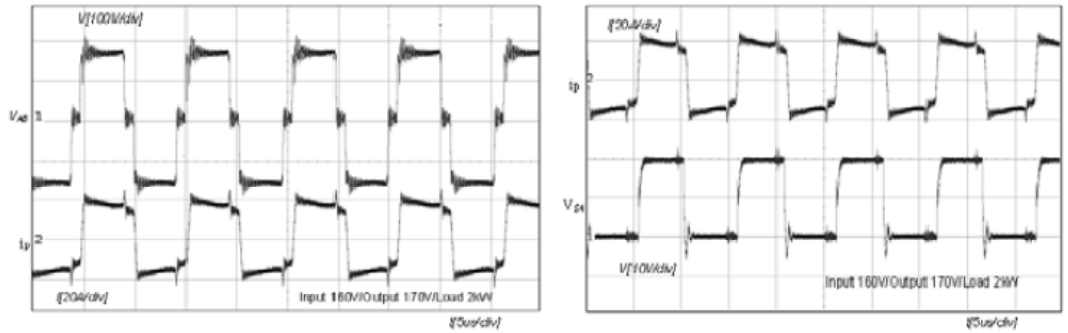


Figure 7: Bridge midpoint voltage waveform and the primary side current waveform

Te lagging leg Q3 has achieved ZVS soft switching. V_{Q3} is driving waveform, V_{S3} is the voltage of switching tube source-drain. As shown in Figure 8, the interior of the oscilloscope is common-grounded, so disturbance will be brought in during the messurement. At this time drive end is chosen to be datumpoint.

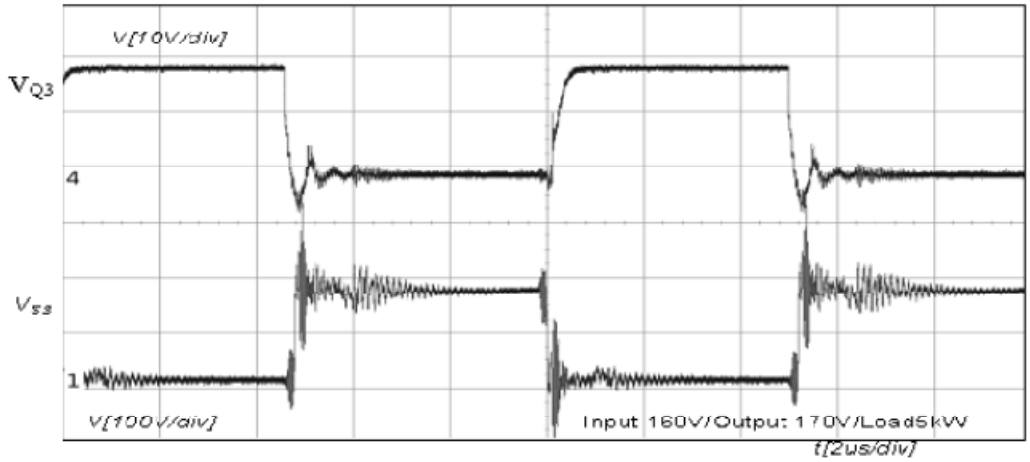


Figure 8: Q3Drive voltage waveform and the drain-source voltage waveform

Figure 9 To clamp voltage waveform rectified, it can be seen from the experimental results that stable voltage rectifier weaken ringing and overshoot phenomenon better to reduce the voltage stress on the rectifier.

Finally, Figure 10 shows the experimentally measured efficiency curve. Comparing with efficiency of the traditional phase-shifted full-bridge converter efficiency, it can be seen under light load the topological transformation efficiency is significantly improved when we use the method this paper tell. However, the efficiency in the full load range of the converter raise by about 2%.

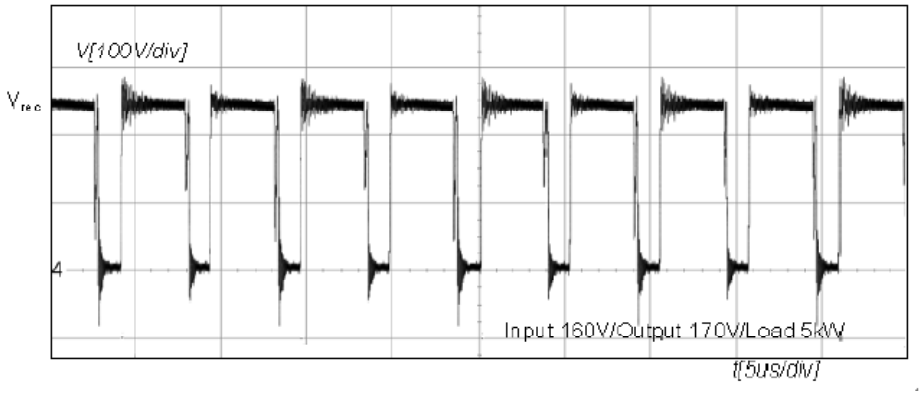


Figure 9: Secondary clamping voltage waveform

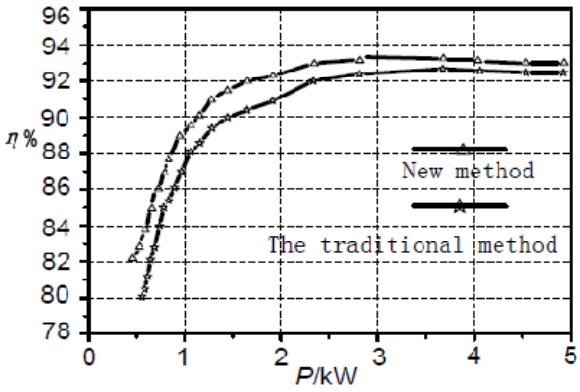


Figure 10: Converter efficiency curve

CONCLUSION

This paper studies the original side adding a coupled inductor, and the secondary side active clamp using phase-shifted full-bridge zero voltage switching PWM converter. In-depth analysis of the phase-shifted full-bridge topology, zero voltage switching PWM converter works. Secondary steady-state voltage clamp capacitance analysis is verified by experimental research phase-shifted full-bridge zero voltage switching PWM converter works. Realizing its wide input voltage range and a large load range switch tube ZVS and rectifier pipe ends of the active clamp snubber circuit. In parallel, it can effectively inhibit rectifier voltage overshoot and ringing, thus effectively reducing the rectifier voltage stress. Conversion efficiency of this article also improved circuit topology than traditional phase-shifted full-bridge circuit to high, especially in the case of light load being more notable.

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